Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**BASE**

**.026”**

**EMITTER**

**.031”**

**Top Material: Al**

**Backside Material: Gold**

**Bond Pad Size: .0045” X .0045”**

**Backside Potential: Collector**

**Mask Ref: G9**

**APPROVED BY: DK DIE SIZE .026” X .031” DATE: 11/17/21**

**MFG: ZETEX THICKNESS .007” P/N: 2N1893**

**DG 10.1.2**

#### Rev B, 7/19/02